REMARKS

Claims 1-85 are currently pending. Claims 12-61, 69-73 and 81-85 have been allowed, claims 1-9, 62-66, and 74-78 stand rejected, and claims 10, 11, 67, 68, 79 and 80 stand objected to. Claims 1, 5, 62, and 74 have been amended. No new matter has been added. Applicant reserves the right to pursue original claims and other claims in this and any other application.

Applicant appreciates the indication of allowability of claims 12-61, 69-73 and 81-85.

Claims 1, 3-5, 7-8, 62, and 64-65 stand rejected under 35 U.S.C. § 102(e) over Shimizu et al. (U.S. Pat. No. 6,628,559)("Shimizu"). Applicant respectfully requests reconsideration of this rejection.

Shimizu discloses a semiconductor memory device having "a refresh time for generating a refresh clock, a refresh executing circuit for sequentially refreshing a plurality of memory cells part by part on the basis of the cycle of the refresh clock...." (Shimizu, Abstract)

Claim 1 recites, *inter alia*, a memory refresh circuit comprising "a control circuit for conducting a memory refresh operation, for monitoring a memory device, and for indicating when said refresh operation is complete based on said monitoring of said memory device."

Shimizu fails to disclose or suggest "indicating when said refresh operation is complete based on said monitoring of said memory device." The claimed invention is based on a circuit which dynamically provides a signal indicating when a refresh operation is complete. As noted in an exemplary embodiment of the invention, rather than provide a set time period for a memory refresh to occur, the claimed invention includes a circuit which monitors whether "any of memory devices 530 is currently performing burst self refresh." (Klein, specification ¶ 0028) As result, a refresh complete signal is provided dynamically based on monitoring the memory devices to indicate when none of the memory devices are performing a refresh operation. To the contrary, the invention of Shimizu is based on a timing clock which provides a static, pre-determined time period to complete a refresh operation. (see, for example, Shimizu, Col. 8, lines 8-40). As such, the memory refresh circuit and refresh complete signal of the claimed invention is different from the memory refresh circuit and refresh complete signal of the invention of Shimizu. Therefore, the rejection of claim 1 should be withdrawn.

Claims 3 and 4 depend, directly or indirectly, from claim 1 and incorporate all the limitations thereof, and are allowable for at least the reasons noted above. Therefore the rejection of these claims should be withdrawn.

Claim 5 has a similar limitation as claim 1 and therefore should be allowable for at least the reason noted above. As such, the rejection of claim 5 should be withdrawn.

Claims 7 and 8 depend, directly or indirectly, from claim 5 and incorporate all the limitations thereof, and are allowable for at least the reasons noted above. Therefore the rejection of these claims should be withdrawn.

Claim 62 has a similar limitation as claim 1 and therefore should be allowable for at least the reason noted above. As such, the rejection of claim 62 should be withdrawn.

Claims 64 and 65 depend, directly or indirectly, from claim 62 and incorporate all the limitations thereof, and are allowable for at least the reasons noted above. Therefore the rejection of these claims should be withdrawn.

Claims 2, 6, and 63 stand rejected under 35 U.S.C. § 103(a) over Shimizu in view of Takahashi et al. (U.S. Pat. No. 6,751,144)("Takahashi"). Applicant respectfully requests reconsideration of this rejection.

Takahashi discloses a semiconductor memory device having a refresh control circuit refreshes a memory cell when an address change detection signal is received, where the control circuit uses a timer to control the refresh operation. (Takahashi, Abstract, Col. 13, lines 14-28)

Claims 2, 6, and 63 are dependent from independent claims 1, 5, and 62, respectively, and are allowable for at least the reasons noted above.

Additionally, with respect of claim 1, neither Shimizu nor Takahashi, either separately or in combination, disclose or suggest "a control circuit for ... "indicating when said refresh operation is complete based on said monitoring of said memory device." Nor is there provided in either Shimizu or Takahashi the motivation or suggestion to combine the teachings of each respective invention to achieve the claimed invention as both inventions teach refresh operations based on time clock. Therefore, as claim 2 is dependant on claim 1, the rejection of claim 2 should be withdrawn.

Claims 6 and 63 have a similar limitation as claim 1 and are allowable for the reasons noted above.

Claims 9 and 66 stand rejected under 35 U.S.C. § 103(a) over Shimizu in view of Tsukude et al. (U.S. Pat. No. 6,697,910)("Tsukude"). Applicant respectfully requests reconsideration of this rejection.

Tsukude discloses semiconductor memory device with "a refresh circuit [that] outputs a refresh command signal for executing refresh operation." (Tsukude, Abstract) In Tsukude, the refresh operation is based upon a specified period of time. (Tsukude, Col. 7, lines 30-36)

Claims 9 and 66 are dependent from independent claims 5 and 62, respectively, and are allowable for at least the reasons noted above. Additionally, with respect of claim 5, neither Shimizu nor Tsukude, either separately or in combination, disclose or suggest "indicating when said refresh operation is complete based on said monitoring of said memory array." Nor is there provided in either Shimizu or Tsukude the motivation or suggestion to combine the teachings of each respective invention to achieve the claimed invention as both inventions deal with static operations based on pre-determined time periods. Therefore, as claim 9 is dependant on claim 5, the rejection of claim 9 should be withdrawn.

Claim 66 has a similar limitation as claim 1 and is allowable for the reasons noted above.

Claims 74 and 76-77 stand rejected under 35 U.S.C. § 103(a) over Shimizu in view of Moazzami et al. (U.S. Pat. No. 5,270,967)("Moazzami"). Applicant respectfully requests reconsideration of this rejection.

Moazzami discloses refreshing a memory array having ferroelectric capacitors by "impressing a voltage across the ferroelectric capacitor, which voltage is higher than that which the capacitor experiences during normal operation." (Moazzami, Abstract) Further, Moazzami discloses a refresh operation controlled by a processing system. (Moazzami, Col 2, line 20 – Col. 3, line 10)

Claim 74 recites, *inter alia*, processor system, comprising "a processor, and a memory device, comprising: a memory array; and a refresh circuit for controlling a refresh operation of the memory array, for monitoring said memory array, and for indicating when said refresh operation is complete based on said monitoring of said memory array."

Neither Shimizu nor Moazzami, separately or in combination, disclose or suggest "indicating when said refresh operation is complete based on said monitoring of said memory array." Nor is there provided in either Shimizu or Moazzami the motivation or suggestion to combine the teachings of each respective invention to achieve the claimed invention as Shimizu discloses static refresh timing and Moazzami discloses a processor controlling a refresh operation. As such, the rejection of claim 74 and 76-77 should be withdrawn.

Claim 75 stands rejected under 35 U.S.C. § 103(a) over Shimizu in view of Moazzami and Takahashi. Applicant respectfully requests reconsideration of this rejection.

Claim 75 depends from claim 74 is allowable for at least the reason noted above. Furthermore, neither Shimizu nor Moazzami nor Takahashi, separately or in combination, disclose or suggest "indicating when said refresh operation is complete based on said monitoring of said memory array." Nor is there provided in either Shimizu or Takahashi or Moazzami the motivation or suggestion to combine the teachings of each respective invention to achieve the claimed invention. Therefore, the rejection of claim 75 should be withdrawn.

Claim 78 stands rejected under 35 U.S.C. § 103(a) over Shimizu in view of Moazzami and Tsukude. Applicant respectfully requests reconsideration of this rejection.

Claim 78 depends from claim 74 is allowable for at least the reason noted above. Furthermore, neither Shimizu nor Moazzami nor Tsukude, separately or in combination, disclose or suggest "indicating when said refresh operation is complete based on said monitoring of said memory array." Nor is there provided in any one of Shimizu, Moazzami, or Tsukude the motivation or suggestion to combine the teachings of each respective invention to achieve the claimed invention. Therefore, the rejection of claim 78 should be withdrawn.

The Office Action states that claims 10-11, 67-68, and 79-80 stand objected to as being dependent upon a rejected base claim. The Applicant respectfully suggests that the base claims are allowable for at least the reasons noted above and therefore claims 10-11, 67-68, and 79-80 are also allowable.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Michael A. Weinstein
Registration No.: 53,754
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant